On the design of a 55 GHz Si/SiGe HBT frequency doubler operating close to f_{max}

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Abstract

In this paper we present for the first time experimental results on a frequency doubler using a Si/SiGe HBT as the non-linear element. Despite the high output operating frequency being close to f_{max}, 67 GHz, for the Si/SiGe HBT, the conversion efficiency in a not completely optimised circuit was found to be better than -12 dB. The 3 dB bandwidth for the doubler was about 7.4%. These results are found to be comparable to an HFET doubler operating equally close to its f_{max}. The results agree well with the prediction for the multiplier from a developed physics-based large-signal HBT model. Prediction by the model using harmonic balance simulation at 55 GHz shows that a conversion efficiency for the Si/SiGe HBT of about 5 dB can be expected from future optimised circuits.

Introduction

Silicon based active devices such as Si/SiGe Heterojunction Bipolar Transistors (HBT) have shown to have great potentials of performance where devices with a maximum frequency of oscillation (f_{max}) of 80 GHz have been implemented in circuits [1] and f_{max} of 160 GHz has been reached recently in common emitter configuration for single devices [2]. Thus f_{max} for state of the art Si/SiGe HBTs are well above the important operating frequencies to be used in automotive applications such as car - car communication and car radar. In order to evaluate the feasibility of this technology for applications at millimeterwave frequencies, an active second harmonic 55 GHz frequency doubler using an Si/SiGe HBT as the active device has been designed.

Design of the Doubler

The circuit structure used in the implementation of the doubler has been chosen to be Coplanar Waveguide (CPW) due to the large impedance range and lower dispersion that can be achieved for this circuit technology compared to microstrip and also due to the practical advantage of not having to use viaholes for ground connection. This is of particular importance in the case of monolithic integration of circuits [3]. The monolithic matching circuits for the multiplier, implemented on high-ohmic silicon, have been centred around 50 ohm transmission-lines in order to reduce the complexity in the number of circuits needed to design the doubler.

To ensure a good understanding on how to realise the passive structures, consisting of shorts, opens, crosses and MIM-capacitors, test circuits have been designed using E-M-field simulators from Hewlett Packard [4] and then fabricated. Results from measurements on the passive structures conform well with simulated data up to at least 40 GHz (current limit of the used measurement equipment). For the doubler circuit itself, the HBT was bonded into the monolithic passive circuitry using preformed beamleads, included in the electrical design. The layout of the 55 GHz doubler is shown in Fig.1. The input and output matching to 50 ohms were achieved using stub circuits where the stubs were terminated in shorts (MIM-capacitors). On the output, a filter (consisting of open quarter-wave stubs) was used to suppress the fundamental frequency.

A new physics-based large-signal Si/SiGe HBT model has been derived and used in the design of the frequency doubler. It employs a modified Ebers-Moll model which has technological data as input parameters. The heterojunction is accounted for by treating the different kinds of injections separately, which simplifies modelling of for example the current dependency of β.

With the use of fitting of given input parameters, within realistic limits, to measurements such as Gummel- and IV-plots in conjunction with S-parameters at different bias points, it is possible to model the transistors behaviour throughout the interesting region of operation with sufficient accuracy.

Measurements and Discussion

The measurement set-up for the evaluation of the fabricated doubler comprised of a HP8510C vector network analyser for S-parameter measurements. A synthesised sweeper together with a power amplifier was used for the power measurements. The circuit was contacted on input and output side using coplanar probes. The output power was measured using a waveguide V-band power-sensor in order to further suppress the fundamental frequency, being below the cut-off frequency of the waveguide.

The measured frequency doubler showed a conversion efficiency of better than -12 dB at an input power of 1.2 dBm and a DC-bias of 4 V and 3 mA, see Fig. 2. These results are found to be comparable to an HFET doubler operating equally close to its f_{max} [5]. The 3 dB power-bandwidth for the multiplier was measured to be about

7.4%, see Fig 3. In Fig. 3 is also shown the calculated conversion efficiency for the doubler using the derived HBT-model and the calculated impedances for the input and output embedding circuits. The good agreement between theory and experiments makes it possible to predict the conversion behaviour for different HBT devices and improving the design of the doubler.

The multiplier was originally designed for a Si/SiGe HBT (here called DT9502) having a different doping profile, thus having somewhat different S-parameters compared to the used device (here called 3147A1) which was available at the time of implementation. The difference in S-parameters between the devices implied that the used device (3147A1) is not optimally matched for working in this frequency multiplier. The effect of this difference in transistor behaviour can be seen in Fig. 3 where the doubler structure has been simulated using both the DT9502 and 3147A1 as active device.

Preliminary Harmonic-Balance simulations with the new transistor show that a conversion gain of about 5 dB can be expected if optimised matching circuits are employed.

Conclusion

A frequency doubler for 55 GHz with a conversion efficiency of better than -12 dB operating at an output frequency near f_{max} for the device has been designed. By improving the matching circuits to the transistor, an enhancement in conversion of upto 17 dB can be expected. This does not put any demands on improved performance of the transistor itself.

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FIGURES

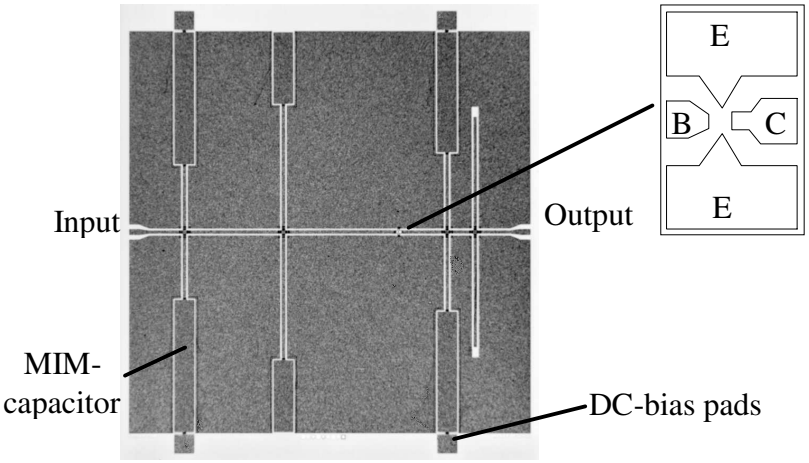

Fig. 1. The fabricated doubler circuit. A schematic of the transistor is shown on the right.

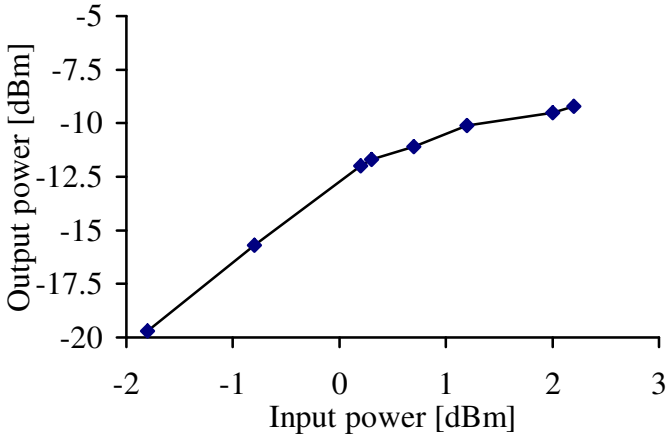

Fig. 2. Measured output power at 54.5 GHz versus source power at fundamental frequency for the doubler circuit.

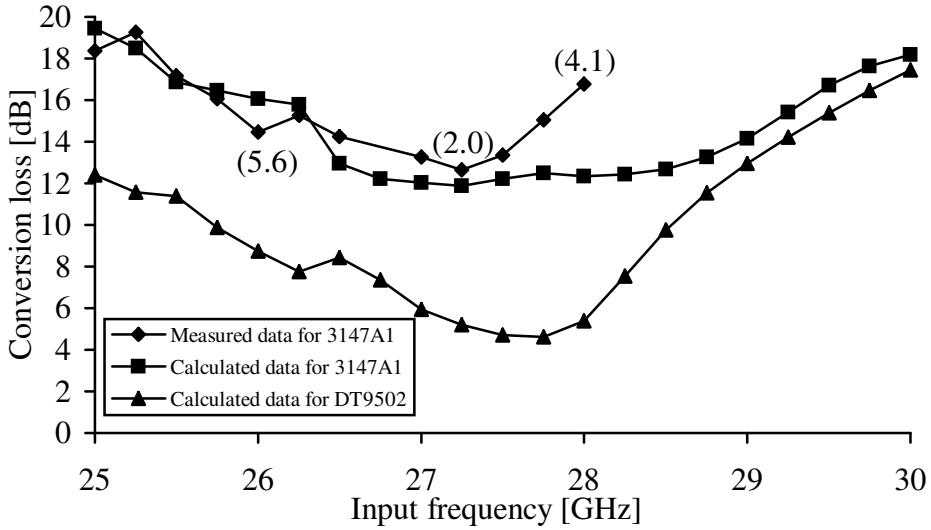

Fig. 3. Conversion loss versus frequency for the doubler circuit. Numbers within parenthesis depict source power at the input.